WHAT IS CLAIMED IS:

1. A phase-locked loop (PLL) lock detector circuit for detecting a lock or unlock state of a PLL circuit, the PLL lock detector circuit comprising:

a synchronization circuit for synchronizing a lock window signal with a reference frequency signal, the lock window signal resulting from dividing the reference frequency signal by a predetermined number;

a rising edge detection circuit for receiving an output signal of the synchronization circuit and an error signal, and for outputting a state of the error signal at a rising edge of the output signal of the synchronization circuit, the error signal indicating a phase difference between the lock window signal and a signal resulting from dividing an output signal of the PLL circuit by a predefined number;

a falling edge detection circuit for receiving the error signal and an inverted lock window signal and for outputting a state of the error signal at a rising edge of the inverted lock window signal; and

a logic circuit for performing an AND operation on an output signal of the rising edge detection circuit and an output signal of the falling edge detection circuit, and for

outputting a signal indicating the lock or unlock state of the PLL circuit.

2. The PLL lock detector circuit of claim 1, wherein the synchronization circuit comprises a delay flip-flop having a control clock terminal, a delay input terminal, an output terminal and an inverting output terminal, the reference frequency signal is applied to the control clock terminal, and the lock window signal is applied to the delay input terminal.

3. The PLL lock detector circuit of claim 1, wherein the rising edge detection circuit comprises a delay flip-flop having a control clock terminal, a delay input terminal, an output terminal and an inverting output terminal, the output of the synchronization circuit is applied to the control clock terminal, and the error signal is applied to the delay input terminal.

4. The PLL lock detector circuit of claim 1, wherein the falling edge detection circuit comprises a delay flip-flop having a control clock terminal, a delay input terminal, an output terminal and an inverting output terminal, the inverted lock window signal is applied to the

control clock terminal, and the error signal is applied to the delay input terminal.

5. The PLL lock detector circuit of claim 1, further comprising an inverter for inverting the lock window signal to output the inverted lock window signal.

6. A method of detecting a lock or unlock state of a phase-locked loop (PLL) circuit, comprising the steps of:

synchronizing a reference frequency signal with a lock window signal to output a resulting signal of the synchronization, the lock window signal resulting from dividing the reference frequency signal by a predetermined number;

detecting a state of an error signal at a rising edge of the resulting signal of the synchronization, the error signal indicating a phase difference between the lock window signal and a signal that results from dividing an output signal of the PLL circuit by a predefined number;

detecting a state of the error signal at a rising edge of an inverted lock window signal; and

performing an AND operation with respect to the detected states of the error signal, to determine the lock or unlock state of the PLL circuit.

7. The method of claim 6, wherein said step of synchronizing the reference frequency signal with the lock window signal comprises the step of inputting the lock window signal and the reference frequency signal to a data input and a clock input of a flip flop, respectively, to obtain the resulting signal of the synchronization from an output of the flip flop.

8. The method of claim 6, wherein said step of detecting the state of the error signal at the rising edge of the resulting signal of the synchronization comprises the step of inputting the error signal and the resulting signal of the synchronization to a data input and a clock input of a flip flop, respectively, to obtain the state of the error signal at the rising edge of the resulting signal of the synchronization from an output of the flip flop.

9. The method of claim 6, wherein said step of detecting the state of the error signal at the rising edge of the inverted lock window signal comprises the step of inputting the error signal and the lock window signal to a data input and a clock input of a flip flop, respectively, to obtain the state of the error signal at the rising edge

of the inverted lock window signal output from an output of the flip flop.

10. A phase-locked loop (PLL) lock detector circuit for detecting a lock or unlock state of a PLL circuit, the PLL lock detector circuit comprising:

a synchronization circuit for synchronizing a lock window signal with a reference frequency signal, the lock window signal resulting from dividing the reference frequency signal by a predetermined number;

a detection circuit for receiving an output signal of the synchronization circuit and an error signal, for outputting a state of the error signal at a rising edge of the output signal of the synchronization circuit, for receiving an inverted lock window signal and for outputting a state of the error signal at a rising edge of the inverted lock window signal, the error signal indicating a phase difference between the lock window signal and a signal resulting from dividing an output signal of the PLL circuit by a predefined number; and

a logic circuit for performing an AND operation with respect to the detected states and for outputting a signal indicating the lock or unlock state of the PLL circuit.

11. The PLL lock detector circuit of claim 10, wherein said detection circuit comprises:

a rising edge detection circuit for receiving the output signal of the synchronization circuit and the error signal, and for outputting the state of the error signal at the rising edge of the output signal of the synchronization circuit; and

a falling edge detection circuit for receiving the error signal and the inverted lock window signal and for outputting the state of the error signal at the rising edge of the inverted lock window signal.

12. The PLL lock detector circuit of claim 10, wherein the synchronization circuit comprises a flip-flop having a control clock terminal, a data input terminal, an output terminal and an inverting output terminal, the reference frequency signal is applied to the control clock terminal, and the lock window signal is applied to the data input terminal.

13. The PLL lock detector circuit of claim 11, wherein the rising edge detection circuit comprises a flip-flop having a control clock terminal, a data input terminal, an output terminal and an inverting output terminal, the output

of the synchronization circuit is applied to the control clock terminal, and the error signal is applied to the data input terminal.

14. The PLL lock detector circuit of claim 11, wherein the falling edge detection circuit comprises a flip-flop having a control clock terminal, a data input terminal, an output terminal and an inverting output terminal, the inverted signal of the lock window signal is applied to the control clock terminal, and the error signal is applied to the data input terminal.